IFW AF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

GARY P. MORRISON ET AL.

Serial No. 10/034,827 (TI-31373)

Filed January 3, 2002

For: CHIP-SCALE PACKAGES STACKED ON FOLDED INTERCONNECTOR FOR VERTICAL ASSEMBLY ON SUBSTRATES

Art Unit 2827

Examiner James M. Mitchell

Customer No. 23494

Mail Stop Appeal Brief-Patents
Director of the United States
Patent and Trademark Office
P. O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING OR TRANSMISSION UNDER 37 CFR 1.8

I hereby certify that the attached document is being deposited with the United States Postal Service with sufficient postage for First Class Mail in an envelope addressed to Director of the United States Patent and Trademark Office, P.O. Box 1450,, Alexandria, VA 22313-1450 or is being facsimile transmitted on the date indicated below:

8-23-04

Jay M. Cantor, Reg. No. 19,906

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences.

STATUS OF CLAIMS

This is an appeal of claims 2, 4 to 10, 12, 15, 17, 18, 20 and 23, all of the rejected claims. No claims have been allowed. Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

An amendment was filed after final rejection and was not entered for purposes of appeal for reasons which cannot be understood since the amendments were clearly cosmetic in nature.

SUMMARY OF INVENTION

The invention relates to a semiconductor assembly and to a method of making a semiconductor assembly having a strip-like flexible interconnector (101) of electrically insulating material having first (102) and second (103) surfaces, the interconnector having on the first surface electrically conductive lines (104) for connecting a plurality of separately encapsulated semiconductor devices (108) formed on the first surface adjacent to each other. The interconnect further has electrically conductive paths extending through the interconnector (page 14, line 3) from the first surface to the second surface, forming electrical ports on the second surface. The ports have first (105) and second (106) pluralities of ports, the first plurality of ports spaced apart by less, center to center, than the second plurality of ports are spaced apart, center to center (page 7, lines 16-20). The interconnector is folded so that the adjacent separately encapsulated semiconductor devices are stacked on top of each other (Figs. 1D to 1H and 2D to 2I). At least one additional un-encapsulated semiconductor device (133) has a plurality of first electrical coupling members attached to the first plurality ports and a plurality of second electrical coupling members attached to the second plurality ports which are suitable for attachment to other parts (134).

ISSUE

The sole issue on appeal is whether claims 2, 4,to 10, 12, 15, 17, 18, 20 and 23 are anticipated by Inaba (JP 2001-217388) under 35 U.S.C. 102(e)

GROUPING OF CLAIMS

The claims stand or fall together.

ARGUMENT

Claims 2, 4, to 10, 12, 15, 17, 18, 20 and 23 were rejected as being anticipated by Inaba (JP 2001-217388) under 35 U.S.C. 102(e). The rejection is without merit as will be demonstrated since the Inaba reference is not available as a reference in this application.

The invention was ready for patenting in accordance with the provisions of Pfaff v. Wells Electronics, 525 U.S. 55 (U.S. 1998) as stated in the Declaration Under 37 C.F.R. 1.132 of Jay M. Cantor on a date prior to the publication date of the cited and applied Japanese reference. Accordingly, the Japanese reference is not applicable under 35 U.S.C. 102 in the subject application and the rejection is without merit for that reason.

As stated in the Declaration of Jay M. Cantor, applicants (appellants herein), submitted a patent disclosure for their subject invention or discovery and for the claimed subject matter of the subject application and that it was "ready for patenting" in accordance with the requirements of 35 U.S.C. 102 prior to the effective date of the cited Inaba Japanese publication number 2001-217338, published October 10, 2001 according to the Patent Abstracts of Japan. The invention disclosure attached to the above-noted declaration is dated as received by the Texas Instruments Patent Department prior to the publication date of the above-noted Japanese reference and was accordingly submitted by appellants herein

to the Texas Instruments Patent Department prior to the publication date of the above-noted Japanese reference. Also, Provisional Patent Application number 60/258,525, which, on information and belief, was prepared at least in part from the above-noted invention disclosure and for which priority was not granted, is substantially identical to the subject application and was filed in the name of appellants herein on December 28, 2000, this date being prior to the publication date of the above-noted Japanese reference.

In accordance with the decision by the United States Supreme Court in Pfaff v Wells Electronics, 525 U.S. 55 (U.S. 1998), the meaning of the term "invention" was specifically defined as it applies to 35 U.S.C.

It is clear from reading 35 U.S.C. that the word "invention" in the statute "does not contain any express requirement that an invention must be reduced to practice" as stated in Pfaff and even in section 102(g) where the conception and reduction to practice are specifically mentioned, there is no requirement that these be the only factors considered. If follows, first, that 35 U.S.C. nowhere defines "invention" by a determination solely of the questions of reduction to practice or conception with diligence up to a reduction to practice (actual or constructive). While a proper showing of a reduction to practice or conception with diligence up to a reduction to practice does establish "invention" under 35 U.S.C, there is nothing in 35 U.S.C. which limits the definition of invention to only those factors. This is confirmed in Pfaff wherein the Court rejected the longstanding precedent set forth above by stating

> [III] "Pfaff nevertheless argues that longstanding precedent buttressed by the strong interest in providing inventors with a clear standard identifying the onset of the 1-year period, justifies a special interpretation of the word 'invention' as used in § 102(b). We are persuaded that this nontextual argument should be rejected."

As stated in the opinion in defining the term "invention", the Court states that:

"Thus petitioner's argument calls into question the standard applied by the Court of Appeals, but it does not persuade us that it is necessary to engraft a reduction to practice element into the meaning of the term 'invention' as used in § 102(b)."

The Court further states:

> "The word 'invention' must refer to a concept that is complete, rather than merely one that is 'substantially complete.' It is true that reduction to practice ordinarily provides the best evidence that an invention is complete. But just because reduction to practice is sufficient evidence of completion, it does not follow that proof of reduction to practice is necessary in every case. Indeed, both the facts of the Telephone Cases and the facts of this case demonstrate that one can prove that an invention is complete and ready for patenting before it has actually been reduced to practice."

The Court concluded that the on-sale bar applies when two conditions are satisfied, the first condition not being applicable in this case because it relates to conditions of sale. However, the second condition relates to the definition of "invention" and states:

> "Second, the invention must be ready for patenting. That condition may be satisfied in at least two ways: by proof of reduction to practice before the critical date; or by proof that prior to the critical date the inventor had prepared drawing or other descriptions of the invention that were sufficiently specific to enable a person skilled in the art to practice the invention. In this case the second condition of the on-sale bar is satisfied because the drawing Pfaff sent to the manufacturer before the critical date fully disclosed the invention" (underline not in original)

It follows that an invention disclosure is provided when it contains "prepared drawing or other descriptions of the invention that were sufficiently specific to enable a person skilled in the art to practice the invention".

In the present case, the disclosure form attached to the Declaration of Jay M. Cantor contains the claimed subject matter of the subject application as does the provisional application referred to above. In fact, in the case of the provisional application, the submission was substantially identical to that of the subject application. The subject application must be considered to be "ready for patenting" since there is no

rejection of record stating that the claimed invention is not adequately disclosed, nor should there be. It follows that even if it be erroneously argued that the attached form does not contain the claimed invention "ready for patenting" then the provisional application contains must contain a disclosure which was "ready for patenting" as defined by the Supreme Court in Pfaff and that appellants are entitled to rely at least upon the date of submission of the attached disclosure form to the assignee patent department. (and possibly an earlier date if it can be established) and/or the filing date of the above referenced provisional application.

The Examiner, in the Advisory Action, has substantially ignored that which is stated in Pfaff other than to state that "PFAFF v. Wells Electronics is nonanalagous (sic) in that it dealt with the issue of infringement not this application's issue of the requirements needed to enable applicant to swear behind a reference". While the Pfaff case does deal with infringement, the requirements of 35 U.S.C.102 are in no way altered because patentability is being tested in an infringement action as opposed to a proceeding before the Patent and Trademark Office. There is not one section 102 for infringement actions and another section 102 for prosecution before the Patent and Trademark Office. If there be such a difference, the undersigned has not found such difference in 35 U.S.C. and, clearly, the examiner has nowhere pointed out such a difference in the statute or in the law. Section 102 is and must be interpreted in the same manner for all questions of patentability of any type and, for this reason, the above-referenced Pfaff decision of the Supreme Court of the United States is controlling and must be followed by the Patent and Trademark Office. If follows that the above-noted Japanese reference is not available under 35 U.S.C 102 in this case and that the rejection must therefore be reversed.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,

Jay M. Cantor
Reg. No. 19906
(301) 424-0355

APPENDIX

The claims on appeal read as follows:

2. The assembly according to Claim 15 wherein said un-encapsulated semiconductor device is an integrated circuit chip having an active and a passive surface, said first coupling members attached to said active surface.

4. The assembly according to Claim 15 further comprising at least one passive electrical component integrated into said conductive lines on said interconnector.

5. The assembly according to Claim 15 wherein said entry ports are spaced apart less than 100 μm center to center, and said exit ports are spaced apart more than 100 μm center to center.

6. The assembly according to Claim 15 wherein said interconnector is a flexible polyimide film.

7. The assembly according to Claim 15 wherein said electrically conductive lines are made of a material selected from a group consisting of copper, copper alloy, or copper plated with tin, tin alloy, silver, or gold.

8. The assembly according to Claim 15 wherein said first and second coupling members are solder balls selected from a group consisting of pure tin, tin alloys including tin/copper, tin/indium, tin/silver, tin/bismuth, tin/lead, and conductive adhesive compounds.

9. The assembly according to Claim 15 wherein said first coupling members are selected from a group consisting of gold bumps, copper bumps, copper/nickel/palladium bumps, and z-axis conductive epoxy.

10. The assembly according to Claim 15 further having an adhesive non-conductive polymer underfilling any spaces between said first coupling members attached to said entry ports under said semiconductor device.

12. The assembly according to Claim 15 further comprising at least one discreet passive electrical component attached to said ports.

15. A semiconductor assembly comprising:

a strip-like flexible interconnector of electrically insulating material having first and second surfaces;

said interconnector having on said first surface electrically conductive lines for connecting a plurality of separately encapsulated semiconductor devices formed on said first surface adjacent to each other;

said interconnect further having electrically conductive paths extending through said interconnector from said first surface to said second surface, forming electrical ports on said second surface;

said ports comprise first and second pluralities, said first plurality (sic) ports spaced apart by less, center to center, than said second plurality ports are spaced apart, center to center;

said interconnector folded so that said adjacent separately encapsulated semiconductor devices are stacked on top of each other;

at least one additional un-encapsulated semiconductor device having a plurality of first electrical coupling members, said first coupling members attached to said first plurality ports; and

a plurality of second electrical coupling members attached to said second plurality ports, said coupling members suitable for attachment to other parts.

17. The method according to Claim 23 further comprising the step of:

integrating at least one passive electrical component into said conductive lines on said interconnector.

18. The method according to Claim 23 further comprising the step of:

underfilling an adhesive non-conductive polymer into any spaces between said first coupling members attached to said entry ports under said semiconductor device.

20. The method according to Claim 23 further comprising the step of:

attaching at least one discreet passive electrical component to said ports.

23. A method of assembling an integrated circuit device, comprising the steps of:

forming electrically conductive lines on a strip-like flexible interconnector of electrically insulating material having first and second surfaces;

forming electrically conductive paths extending through said interconnector from said first surface to said second surface, forming electrical ports on said second surface such that said ports comprise first and second pluralities, said first plurality ports spaced apart less, center to center, than said second plurality ports are spaced apart, center to center;

forming on said first surface a plurality of separately encapsulated semiconductor devices adjacent to each other and connected to said conductive lines;

attaching at least one additional un-encapsulated semiconductor device, having a plurality of first electrical coupling members, to said first plurality ports;

attaching a plurality of second electrical coupling members to said second plurality ports; and

folding said interconnector so that adjacent semiconductor devices are stacked on top of each other.